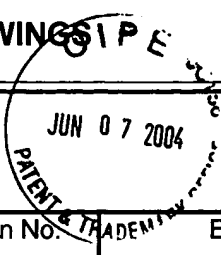


IFW

TRANSMITTAL OF FORMAL DRAWINGS

Docket No.
BUR920040001US1 (17382)

In Re Application Of: **John M. Cohn, et al**



Serial No.
10/709,754

Filing Date
May 26, 2004

Confirmation No.
Unassigned

Examiner
Unassigned

Art Unit
Unassigned

Invention: **FPGA ICE BREAKPOINT/LOGIC EC**

Address to:
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Transmitted herewith are:

2 sheets of formal drawing(s) for this application.

☒ Each sheet of drawing indicates the identifying indicia suggested in 37 CFR Section 1.84(c).


Signature

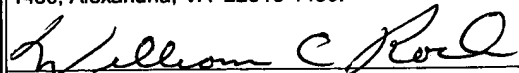
William C. Roch, Esq.
Registration No. 24,972

Dated: **June 3, 2004**

Correspondence Address

Customer No.: 23389

I certify that this document and attached formal drawings
are being deposited on **6/3/04** with the
U.S. Postal Service as first class mail under 37 C.F.R. 1.8
and addressed to the Commissioner for Patents, P.O. Box
1450, Alexandria, VA 22313-1450.


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William C. Roch

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